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NASA TECH BRIEF

Marshall Space Flight Center

High-Performance Schottky Diodes Endure High Temperatures

The problem:

Microwave, GaAs (gallium arsenide) Schottky barrier diodes must have high cutoff frequency to yield high performance. The diodes of this quality, however, have low tolerance to elevated temperature. Because of this two problems are created. One occurs during fabrication: Since the Schottky contacts are sensitive to high temperature, they must be formed after the alloying of the ohmic contacts. The GaAs is fragile, and much of it is lost during the subsequent photoetching steps. The second problem is due to low diode resistance to RF-pulse power burnout. At the high temperatures generated by the RF, contact metals such as gold or platinum are not suitable because much diffusion occurs between these metals and the GaAs.

The solution:

An improved fabrication process and a new aluminum/GaAs coupling are used to produce Schottky diodes that have high cutoff frequencies and can withstand operating temperatures in excess of 500° C.

How it's done:

The fabrication steps are shown in the illustrations. The starting material is a wafer of low-resistivity semiconductor material. A thin epitaxial layer of n-type GaAs is grown on the surface of this material. The typical thickness of this layer is 0.5 to 3.0 μm. Next, a thin layer of insulating material (typically silicon dioxide) is deposited on the epitaxial growth of GaAs to a thickness of 30 μm (see Figure 1).

After the deposition of the insulating layer, openings for the diode junctions are formed in the layer by standard masking and etching techniques (see Figure 2). This is followed by the formation of an Al/Mo/Au Schottky barrier. The barrier is formed by sequential deposition using RF sputtering (see Figure 3). First, an Al metallization is formed in the openings with an overlay over the insulating layer for strong adhesion. Next, a diffusion barrier layer of Mo is formed, followed by a contact layer of Au.

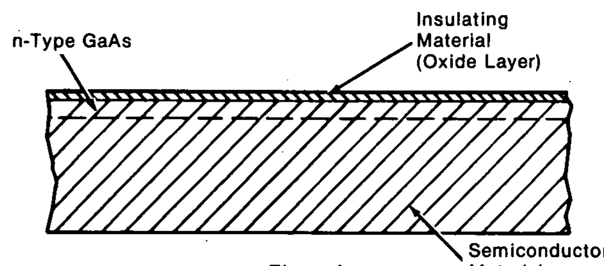

Figure 1

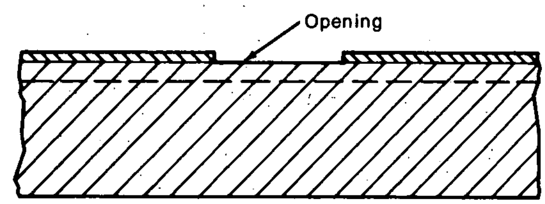

Figure 2

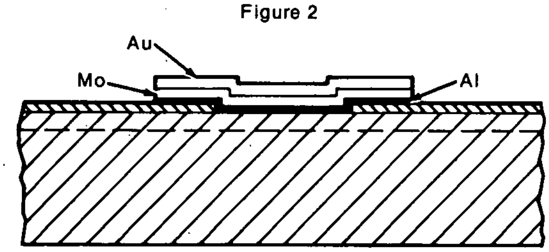

Figure 3

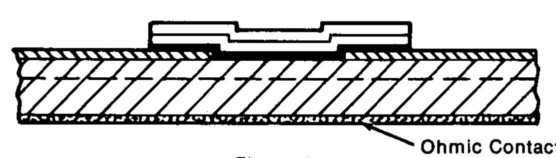

Figure 4

Figures 1 through 4: Diode Fabrication Steps

With most of the processing steps completed, the semiconductor is reduced in thickness from approximately 0.020 in. (0.51 mm) to approximately 0.005 in. (0.13 mm) by lapping and etching its bottom surface. Next, an ohmic contact is formed on this layer by applying a Sn/Ni/Au layer by plating. This layer is then alloyed at temperatures ranging from 450° to 500° C. The wafers are scribed and separated into chips.

Note:

Requests for further information may be directed to:

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Patent status:

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Categories: 01 (Electronics - Components and Circuitry)
04 (Materials)
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